**Switching theory & logic Design**

**UNIT -5**

**MEMORY DEVICES**

A memory is just like a human brain. It is used to store data and instruction. Computer memory is the storage space in computer where data is to be processed and instructions required for processing are stored.

The memory is divided into large number of small parts. Each part is called a cell. Each location or cell has a unique address which varies from zero to memory size minus one.

For example if computer has 64k words, then this memory unit has 64 \* 1024 = 65536 memory location. The address of these locations varies from 0 to 65535.

Memory is primarily of two types

* **Internal Memory** − cache memory and primary/main memory
* **External Memory** − magnetic disk / optical disk etc.



Characteristics of Memory Hierarchy are following when we go from top to bottom.

* Capacity in terms of storage increases.
* Cost per bit of storage decreases.
* Frequency of access of the memory by the CPU decreases.
* Access time by the CPU increases.

## RAM

A RAM constitutes the internal memory of the CPU for storing data, program and program result. It is read/write memory. It is called random access memory (RAM).

Since access time in RAM is independent of the address to the word that is, each storage location inside the memory is as easy to reach as other location &takes the same amount of time. We can reach into the memory at random & extremely fast but can also be quite expensive.

RAM is volatile, i.e. data stored in it is lost when we switch off the computer or if there is a power failure. Hence, a backup uninterruptible power system (UPS) is often used with computers. RAM is small, both in terms of its physical size and in the amount of data it can hold.

RAM is of two types

* Static RAM (SRAM)
* Dynamic RAM (DRAM)

### Static RAM (SRAM)

The word **static** indicates that the memory retains its contents as long as power remains applied. However, data is lost when the power gets down due to volatile nature. SRAM chips use a matrix of 6-transistors and no capacitors. Transistors do not require power to prevent leakage, so SRAM need not have to be refreshed on a regular basis.

Because of the extra space in the matrix, SRAM uses more chips than DRAM for the same amount of storage space, thus making the manufacturing costs higher.

Static RAM is used as cache memory needs to be very fast and small.

### Dynamic RAM (DRAM)

DRAM, unlike SRAM, must be continually **refreshed** in order for it to maintain the data. This is done by placing the memory on a refresh circuit that rewrites the data several hundred times per second. DRAM is used for most system memory because it is cheap and small. All DRAMs are made up of memory cells. These cells are composed of one capacitor and one transistor.

## ROM

ROM stands for Read Only Memory. The memory from which we can only read but cannot write on it. This type of memory is non-volatile. The information is stored permanently in such memories during manufacture.

A ROM, stores such instruction as are required to start computer when electricity is first turned on, this operation is referred to as bootstrap. ROM chip are not only used in the computer but also in other electronic items like washing machine and microwave oven.

Following are the various types of ROM −

### MROM (Masked ROM)

The very first ROMs were hard-wired devices that contained a pre-programmed set of data or instructions. These kind of ROMs are known as masked ROMs. It is inexpensive ROM.

### PROM (Programmable Read Only Memory)

PROM is read-only memory that can be modified only once by a user. The user buys a blank PROM and enters the desired contents using a PROM programmer. Inside the PROM chip there are small fuses which are burnt open during programming. It can be programmed only once and is not erasable.

### EPROM (Erasable and Programmable Read Only Memory)

The EPROM can be erased by exposing it to ultra-violet light for duration of up to 40 minutes. Usually, an EPROM eraser achieves this function. During programming an electrical charge is trapped in an insulated gate region. The charge is retained for more than ten years because the charge has no leakage path. For erasing this charge, ultra-violet light is passed through a quartz crystal window (lid). This exposure to ultra-violet light dissipates the charge. During normal use the quartz lid is sealed with a sticker.

### EEPROM (Electrically Erasable and Programmable Read Only Memory)

The EEPROM is programmed and erased electrically. It can be erased and reprogrammed about ten thousand times. Both erasing and programming take about 4 to 10 ms (millisecond). In EEPROM, any location can be selectively erased and programmed. EEPROMs can be erased one byte at a time, rather than erasing the entire chip. Hence, the process of re-programming is flexible but slow.

### ROM (read-only memory) structure :



Circuit Description

This applet demonstrates the internal structure of a read-only memory or ROM. A rather small memory size of 16 words of 8 bits each is used.

From left to right, the circuit consists of three stages. The first stage, usually called address-decoder in memory circuits, is a standard demultiplexer. For each binary address input pattern, exactly one of thewordlines (horizontal) is activated by the address-decoder. In the example, a 4-to-16 demultiplexer is required to control the 16 wordlines corresponding to the 16 memory addresses.

The memory matrix is the main part of the ROM. For each wordline, a connection is made to those bitlines (vertical) that should be activated for the corresponding memory word. In bipolar technology, simple diodes can be used to make the connections of wordlines to bitlines. However, usually transistors are used to amplify the wordline signal.

In MOS technologies, N-type transistors are preferred, because they are faster than P-type transistors of the same size. The transistor gate is connected to the wordline, drain to the bitline, and the transistor source to Vss (ground). This results in the wired-AND structure shown in the applet. The pullup resistors on each bitline drive the bitline to a weak high voltage (logical H), when no transistors are active. If a transistor is used at the connection of a wordline and bitline, the transistor will conduct whenever the wordline is active, driving the bitline to a low voltage (logical 0).

As N-type transistors are used in the memory matrix, an active bitline is driven to zero voltage, while an inactive bitline remains at (weak) high. Therefore, an additional stage of amplifiers and output buffers is required to generate a strong output signal. The applet uses a single stage of inverters.

All together, the ROM shown in the applet implements the following logical function:

addr A3 A3 A1 A0 D7 D6 D5 D4 D3 D2 D1 D0

15 1 1 1 1 1 1 1 1 1 1 1 1

14 1 1 1 0 0 0 0 0 0 0 0 0

13 1 1 0 1 1 0 0 1 0 0 0 0

12 1 1 0 0 0 0 0 0 0 0 1 1

11 1 0 1 1 0 0 0 0 1 1 1 1

10 1 0 1 0 1 1 1 1 0 0 0 0

9 1 0 0 1 0 0 0 0 0 0 0 0

8 1 0 0 0 0 0 0 0 0 0 0 0

7 0 1 1 1 0 0 0 0 0 0 0 1

6 0 1 1 0 0 0 0 0 0 0 1 0

5 0 1 0 1 0 0 0 0 0 1 0 0

4 0 1 0 0 0 0 0 0 1 0 0 0

3 0 0 1 1 0 0 0 1 0 0 0 0

2 0 0 1 0 0 0 1 0 0 0 0 0

1 0 0 0 1 0 1 0 0 0 0 0 0

0 0 0 0 0 1 0 0 0 0 0 0 0

Due to electrical reasons it is difficult to connect more that a few hundred transistors to one bitline or wordline. Therefore, larger ROMs use a slightly different architecture, with a set of smaller memory blocks instead of one single large memory block. Each memory block uses approximately the same number of wordlines and bitlines (the applet has 16 wordlines and 8 bitlines). For example, a good size for one memory block might consist of 256 wordlines and 256 bitlines. This means that a 64Kx8 bit ROM would be organized internally as a set of (65536x8) / (256x256) = 8 memory blocks. The top 3 address bits select the memory block to use, the next 8 bits select the wordline to use, and the remaining 5 address bits select which part of the memory block output of 256 bits is to be sent to the 8 data outputs.

### RAM (random access memory) structure :



Circuit Description

This applet demonstrates the internal organization of a typical random access memory (RAM). The RAM consists of four main parts, namely

* the memory matrix, built as a 2D-array of 1-bit storage cells,
* the address decoder,
* the input buffer and amplifiers
* the output buffer and amplifiers.

Just play with the RAM inputs (address, data, nChipSelect, and nWriteEnable) and try to write data to the memory cells. You can also check the next three applets for predefined animation sequences:

* [standard write-cycles](https://tams-www.informatik.uni-hamburg.de/applets/hades/webdemos/40-memories/40-ram/ram-write-animation.html)
* [standard read-cycles](https://tams-www.informatik.uni-hamburg.de/applets/hades/webdemos/40-memories/40-ram/ram-read-animation.html)
* [fast write-cycles](https://tams-www.informatik.uni-hamburg.de/applets/hades/webdemos/40-memories/40-ram/ram-hazard-animation.html)

Also, additional applets are provided to demonstrate the individual sub-components of the RAM:

* [single bit memory cell (latch)](https://tams-www.informatik.uni-hamburg.de/applets/hades/webdemos/40-memories/40-ram/ram-latch.html)
* [address decoder](https://tams-www.informatik.uni-hamburg.de/applets/hades/webdemos/40-memories/40-ram/ram-decoder24.html)
* [bitline buffer](https://tams-www.informatik.uni-hamburg.de/applets/hades/webdemos/40-memories/40-ram/ram-bitline-buffer.html)

In order to minimize the chip size of the RAM, a very small size of each storage cell and an efficient layout and signal routing in the memory matrix is essential. One obvious choice is the use of orthogonal wires to access the memory. The wordlines run horizontally and are enabled to select one word of memory data. The bitlines run vertically and are connected to storage cells of different memory address. In the applet, two separate bitlines are used for each data bit. The left bitline of each pair is used to write data into the storage cell selected by an active wordline, while the right bitline is used to read the data. The RAM shown in the applet stores 4 words of 4-bit each (a 4x4 bit RAM). For each cell, an extra LED is used to visualize the data currently stored in the cell (undefined, 0, or 1).

The two most important types of RAM differ in the choice of the storage cell. In principle, any type of latch or flipflop can be used to build a static random access memory, this is, a memory whose contents remains stored while the circuit is powered. Perhaps the most frequently used cell, the so-called six-transistor cell is a variant of the standard transmission-gate latch. An interactive applet demonstration of the 6T-cell can be found [here](http://tams-www.informatik.uni-hamburg.de/applets/sram/). Besides the use of only six transistors to store one-bit of information, the 6T-cell also allows for a very compact routing of signal wires. In dynamic random access memory (DRAM) chips, the storage cell consists of a single NMOS-transistor and a tiny capacitor. A high or low voltage (charge) on the capacitor is interpreted as a logical 1 or 0 value. Due to leakage, the charge on the capacitor has to be refreshed periodically.

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* [bitline buffer](https://tams-www.informatik.uni-hamburg.de/applets/hades/webdemos/40-memories/40-ram/ram-bitline-buffer.html)

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### Memory Expansion :

### When the size of a desired memory system is larger than the number of locations in the chip being used, then several chips will have to be used to provide the additional memory.

* These additional memory chips must be selected (enabled) with additional address decoding. Most microprocessors will provide up to 16 address lines (64K).
* The LSBs of the address bus are connected directly to the memory chips while the higher order address leads are connected to additional decoder chips.
The outputs of these decoders are used to enable individual memory chips.
* Additional decoders can be connected to the address bus to provide memory for all 64K memory addresses.
* Many memory chips (especially MOS devices) require that the data output lines be buffered in order for them to drive heavy loads.